

Patent Abstracts of Japan

PUBLICATION NUMBER : 06140632
PUBLICATION DATE : 20-05-94

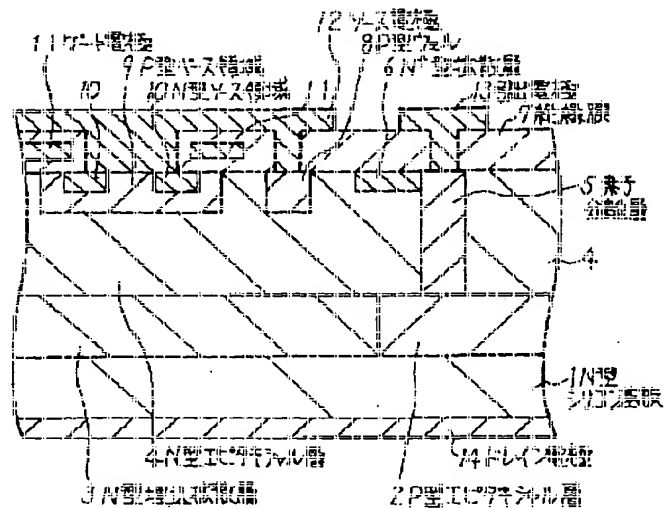
APPLICATION DATE : 27-10-92
APPLICATION NUMBER : 04288048

APPLICANT : NEC CORP;

INVENTOR : KOISHIKAWA YUKIMASA;

INT.CL. : H01L 29/784

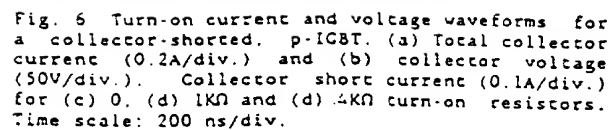
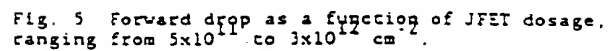
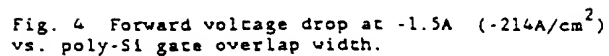
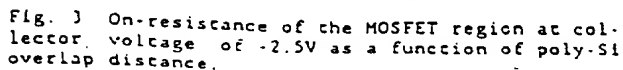
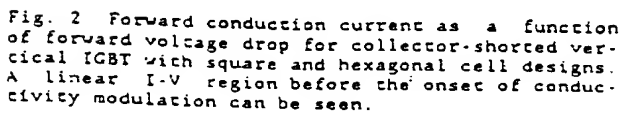
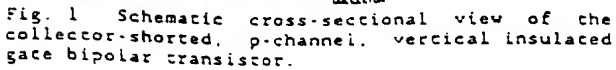
TITLE : SEMICONDUCTOR DEVICE



ABSTRACT : PURPOSE: To prevent the destruction of a vertical type MOSFET due to a counter-electromotive force occurring when an inductive load is driven by providing the vertical type MOSFET of a power IC having a vertical type MOSFET with a built-in diode having a low reverse breakdown voltage.

CONSTITUTION: In a vertical type MOSFET of a power IC in which a p-type epitaxial layer 2 and an n-type epitaxial layer 4 are disposed and the vertical MOSFET and a control circuit are isolated from each other by an element isolation layer 5, a diode having a low reverse breakdown voltage is created by forming an n⁺-type diffusion layer 6 while it is in contact with the element isolation layer 5 within the n-type epitaxial layer 4.

COPYRIGHT: (C) JPO



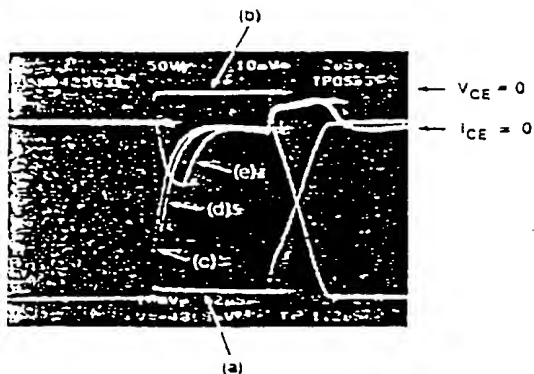


Fig. 7 Turn-on and turn-off current and voltage waveforms for a collector-shortened, p-IGBT. Same current and voltage scales and designations as those in Fig. 6. Time scale: 2 μ s/div.

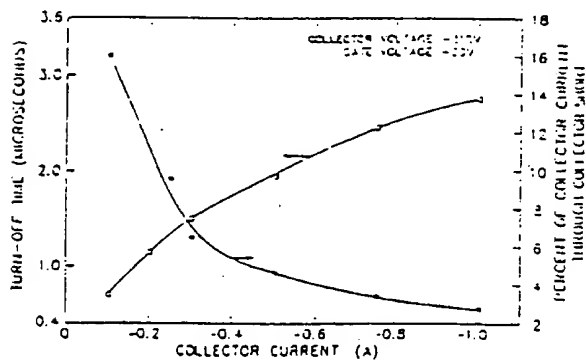


Fig. 8 Turn-off time of collector-shortened vertical IGBT vs. turn-off current for a hexagonal cell design with poly-Si gate overlap of 16 μ m. The fraction of the collector current that goes through the short is also shown to indicate that the increase in turn-off time with increasing current is due to increased minority carrier current.

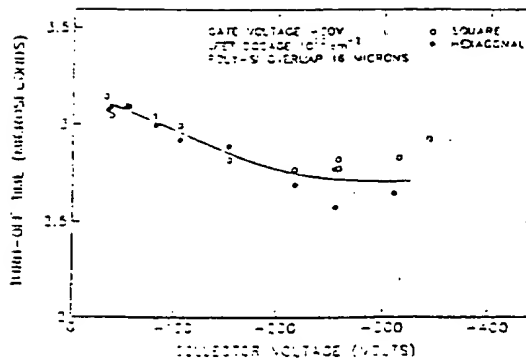


Fig. 9 Turn-off time vs. collector voltage for collector-shortened vertical IGBT with square and hexagonal cell design and poly-Si gate overlap of 16 μ m.

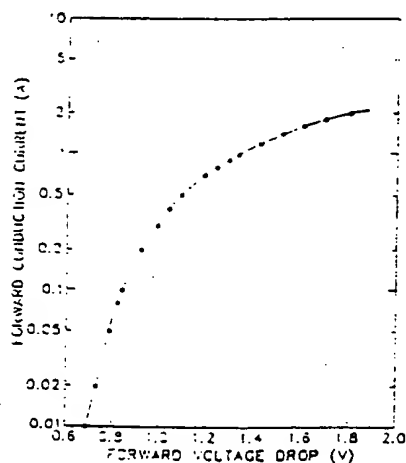


Fig. 10 Forward I-V characteristics for the integral diode formed between the p+ collector short and the deep n+ short in the DMOS cells.